Abstracts

A single chip FSK/ASK 900 MHz transceiver in a standard 0.25 um CMOS technology

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This paper presents a low power consumption single chip FSK/ASK transceiver for half-duplex low datarate communication in the 868-870 MHz band. The IC was processed in a standard 0.25 um CMOS technology, offers a very high level of integration and needs only few external components. The transmit/receive RF front end contains a high efficiency power amplifier, a low noise amplifier (LNA), a double balanced RF mixer and an I/Q mixer for down conversion to an intermediate frequency (IF) of 289 MHz and further to zero IF. The transmit/receive frequency synthesis of 868/1157 MHz is done by a fully integrated switchable frequency range voltage controlled oscillator (VCO), a phase locked loop synthesizer (PLL) and a tunable crystal oscillator used as reference frequency generator as well as FSK modulator. A bandwidth configurable I/Q channel select filter, an I/Q limiter with RSSI generation used also for AM demodulation, a FSK demodulator, a bandwidth configurable data filter and a dataslicer are implemented for further zero IF and baseband analog signal processing. The transceiver can be configured by a 2/3-wire bus interface. Low-drop voltage regulators are implemented to allow supply voltages up to 3.6 V because the maximum allowed voltages for the standard MOS transistors are 2.8 V. The overall current consumption of the transceiver in the receive and transmit mode is 11 mA and 20 mA, respectively. Additionally, a standby mode and idle mode is realized to increase battery lifetime.

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